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Manufacturing with RDRAM* Memory Technology Part III

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Manufacturing with RDRAM Memory Technology

- Production Logistics
  - Handling
  - Packaging

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Chipset Component Handling

- **Chipsets are ESD-sensitive**
  - Same as current chipsets.
  - Be sure to utilize ESD precautions when handling Chipsets and chipset carriers (I.e. tape and reel).
    - » Proper Grounding, clothing, and handling processes.
    - » Chipset Carriers should be unpacked from boxes at ESD Safe Workstations.
    - » Transfer components/T&R using ESD safe trays or materials.
    - » Removed components should be placed in an ESD safe carrier.

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Chipset Component Handling

- **Debug**
  - Don’t surface mount chipsets to a known bad board as this may cause damage to the component.
  - Board Debug - If a chipset component requires a heatsink in your application, a heatsink should be used during debug.
  - mBGA packages require an understanding of the differences in assembly and rework processes. See the “BGA Assembly Development Guide” for information on:
    - Reflow information and tips
    - General rework process and tips
  - Chipset Surface Mount Reference Information

    http://developer.intel.com/design/quality/component/

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Chipset Component Handling

- **Units Handling** -
  - the mBGA balls are softer solder, sliding a unit across a table may cause the array to fail coplanarity limits.
  - Recommended the package be handled like other SMT packages using a quality vacuum pen.
  - Do Not Coin Stack units.

Chipset Component Handling

- **Moisture Sensitivity**
  - PBGA are moisture sensitive packages.
  - The mBGA components are baked and enclosed in a sealed desiccant with a desiccant pouch and humidity indicator card.
  - These mBGA chipsets meet Intel-IPC-786A moisture sensitivity level 4 (MSL-4) or JEDEC Level 4
    - » Up to 72 hours out of bag.
  - Package Delamination may be caused by presence of moisture in the die attach material, solder mask material, mold compound, and substrate.
  - Rebake as per Intel Packaging Handbook.
    - » Low Temp (in T&R) : 192 hours at 40 C, $\leq$ 5% RH.
    - » High Temp (non-T&R): 24 hours at 125 C.

http://www.intel.com/design/packtech/packbook.htm

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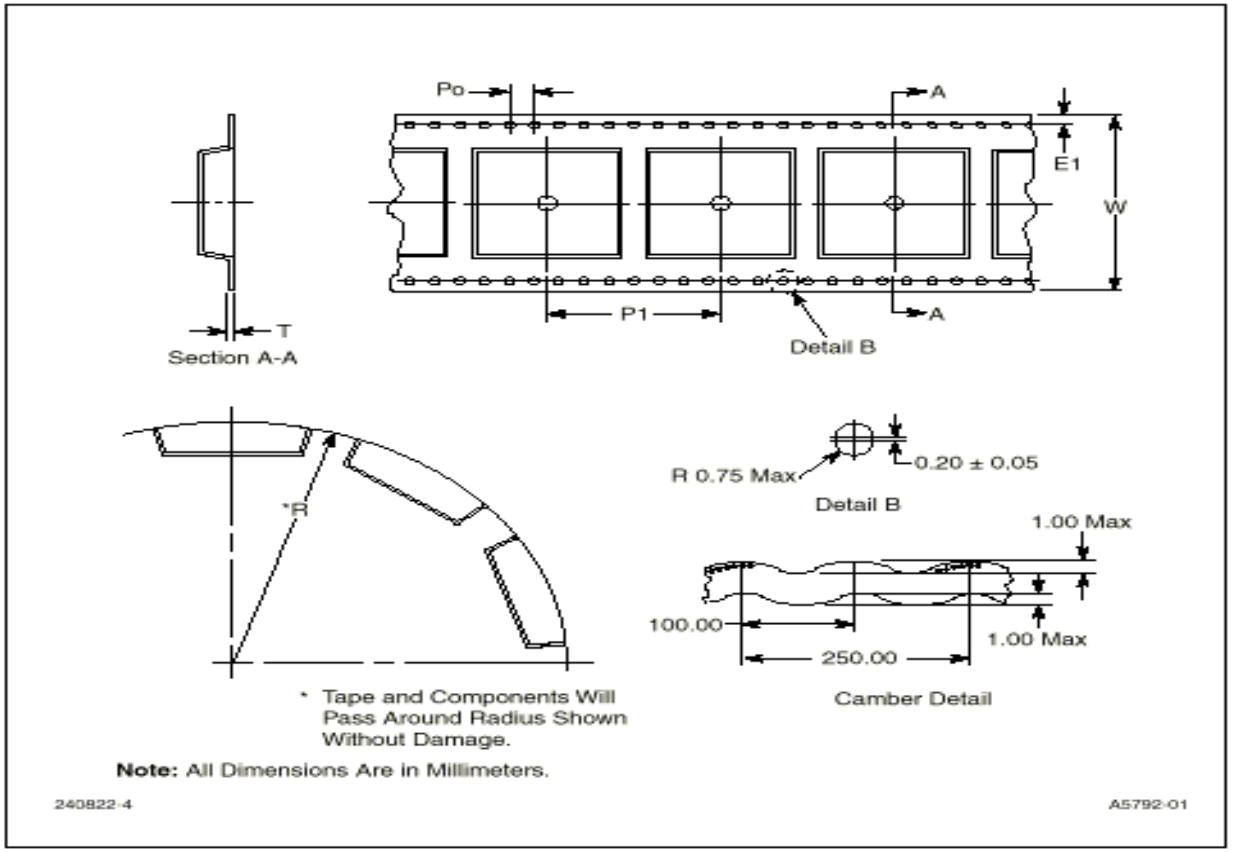
Packaging - Tape and Reel



Package Type	Tape Size	E1	Single/ Double Sprocket	P0	P1	R	T	W	Units/Reel
23 x 23	44mm	1.65-1.85	Double	3.9-4.1	31.9-32.1	89 MIN	.25-.35	43.7-44.3	360
27 x 27	44mm	1.65-1.85	Double	3.9-4.1	31.9-32.1	89 MIN	.25-.35	43.7-44.3	360
35 x 35	56mm	1.65-1.85	Double	3.9-4.1	39.9-40.1	89 MIN	.25-.35	55.7-56.3	360

Packaging - Tape and Reel

Figure 10-10. Carrier Tape Reel

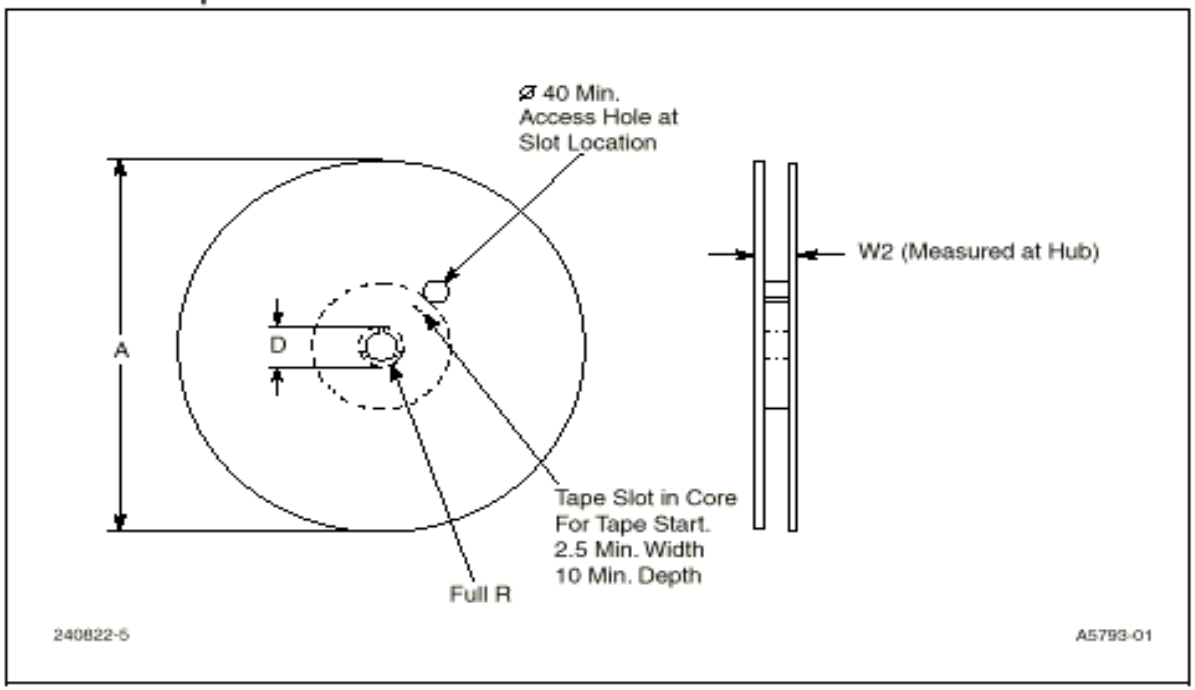


Table 10-27. Carrier Tape Reel Dimensions

Millimeters	12mm	16 mm	24 mm	32 mm	44 mm	56 mm
A Max.	330	330	330	330	330	609
D Min	20.2	20.2	20.2	20.2	20.2	20.2
W2 Max.	16mm	22.4	30.4	38.4	50.4	62.4

NOTE:
1. Dimensions are in millimeters.

Package Handbook URL (Tape and Reel Information) - http://www.intel.com/design/packtech/packbook.htm

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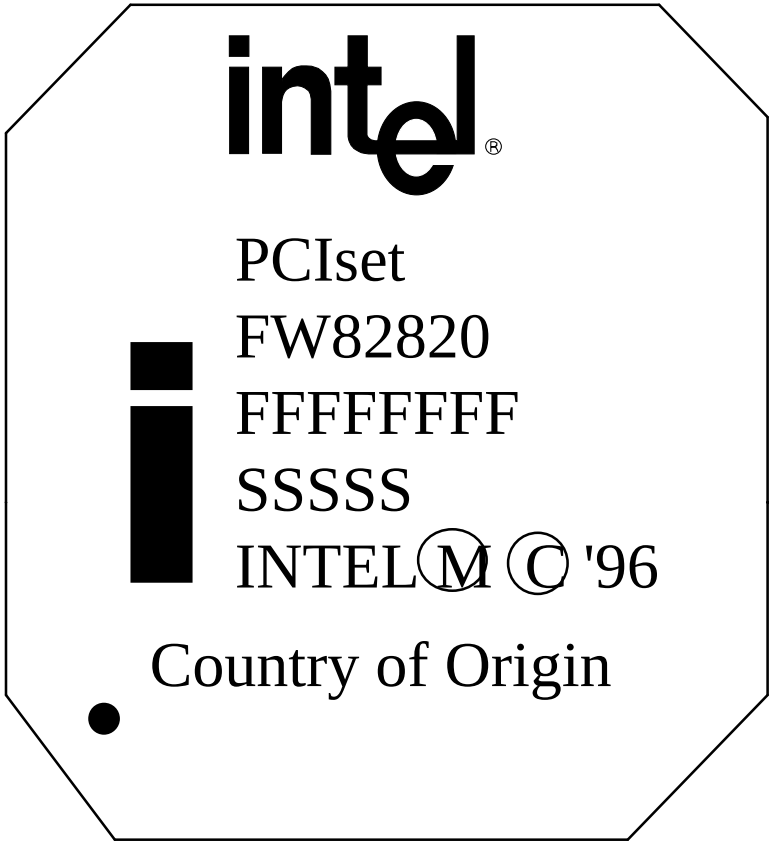
Chipset Marking



- Logo mark
- Product name, S-spec
- Country of origin
- FPO number + identification number
- Pin 1 Indicator
- Legal requirements

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Traceability Information

- **Follows standard Chipset Manufacturing identification marking**
  - » Product code
- **SSSSS= S-spec number**
  - » This is how customers need to identify which version of the Chipset they have.
- **LYWWEFFF =FPO Number** (Used for lot traceability)
  - » L = Test Code
  - » Y = Year
  - » WW = Assembly seal date
  - » E = Assembly code
  - » FFF = serial number